IN THE CLAIMS:

Claims 1 and 2 have been amended herein, and new claims 9 through 12 have been added. Please note that all claims currently pending and under consideration in the referenced application are shown below. Please enter these claims as amended. This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Currently Amended) A substrate for testing semiconductor devices, comprising:
a semiconductor substrate having a dielectric layer on an exposed surface thereof;
at least one conductive trace on said dielectric layer;
a passivation layer over said at least one conductive trace and said dielectric layer; and
a metal-lined via in said passivation layer in electrical communication with said at least one conductive trace, wherein said metal-lined via is sized and configured to temporarily receive a substantially spherical interconnection element attached to a semiconductor device.

2. (Currently Amended) The substrate of claim 1, wherein said metal-lined via is formed of a size and shape to receive approximately 10% to 50% of an overall height of ~~a~~ said substantially spherical interconnection element.

3. (Previously Presented) The substrate of claim 2, wherein said metal-lined via is formed of a size and shape to receive approximately 30% of said overall height of said substantially spherical interconnection element.

4. (Previously Presented) The substrate of claim 1, wherein said metal-lined via includes sloped sidewalls.

5. (Withdrawn) The substrate of claim 1, wherein said metal-lined via includes stepped sidewalls.

6. (Original) The substrate of claim 1, wherein said at least one conductive trace comprises copper.

7. (Original) The substrate of claim 1, wherein said passivation layer comprises polyimide.

8. (Original) The substrate of claim 1, wherein said metal-lined via comprises a metal from the group comprising gold, platinum, palladium, and tungsten.

Please add the following new claims:

9. (New) The substrate of claim 1, wherein said dielectric layer comprises silicon dioxide.

10. (New) The substrate of claim 1, wherein said passivation layer has a thickness of about 20 to 25 microns.

11. (New) The substrate of claim 1, wherein said passivation layer has a thickness of about 100 microns.

12. (New) The substrate of claim 1, further comprising:
at least one additional conductive trace over said passivation layer;
a second passivation layer over said at least one additional conductive trace; and
a second metal-lined via in said second passivation layer in electrical communication with said at least one additional conductive trace.